

Model : M50EA0

Mobile Dothan with INTEL 915PM / ICH6-M Chipset

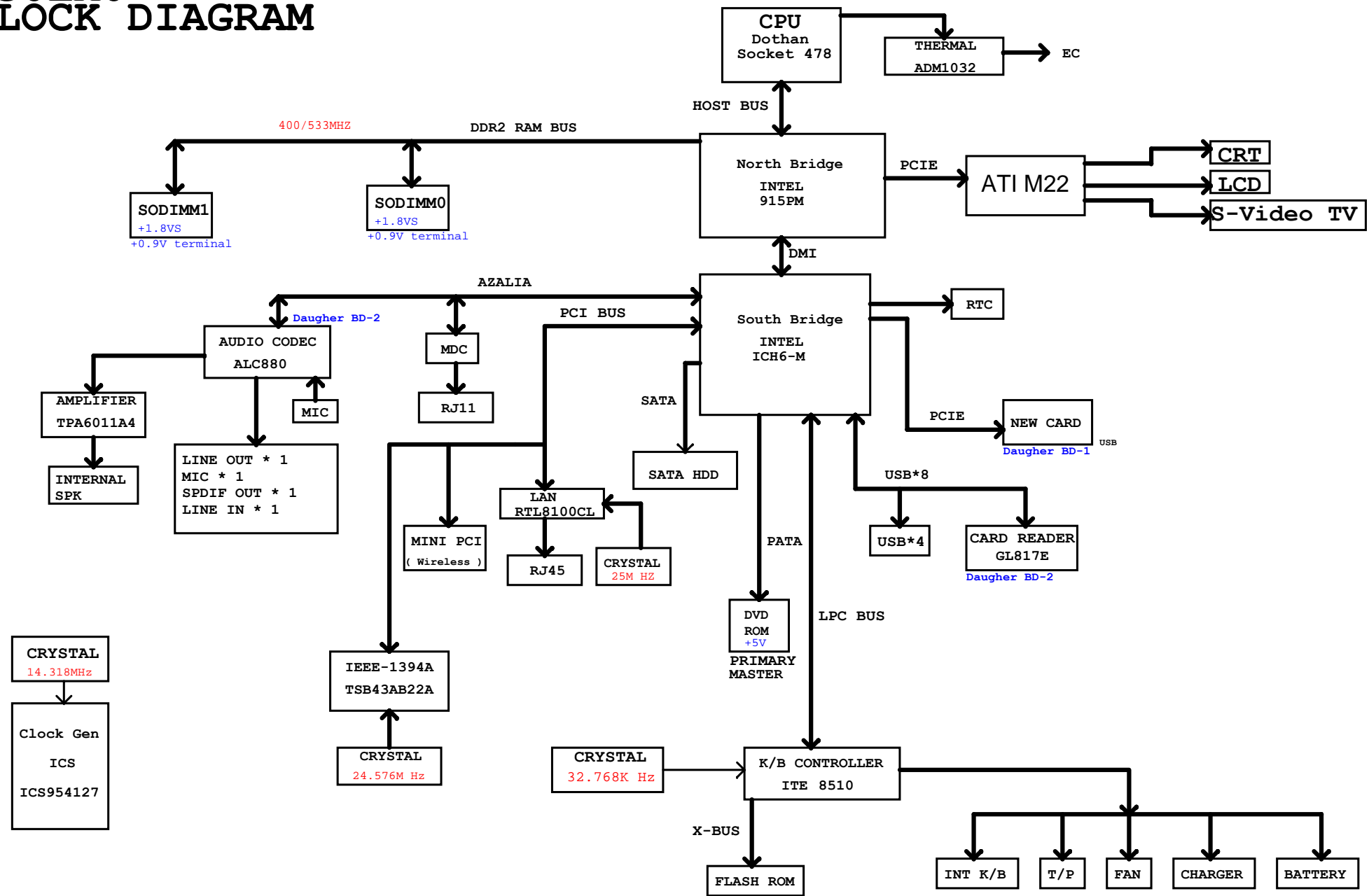
Revision History		
A	11/2004	ORIGINAL RELEASE

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PG03 POWER DIAGRAM & SEQUENCE
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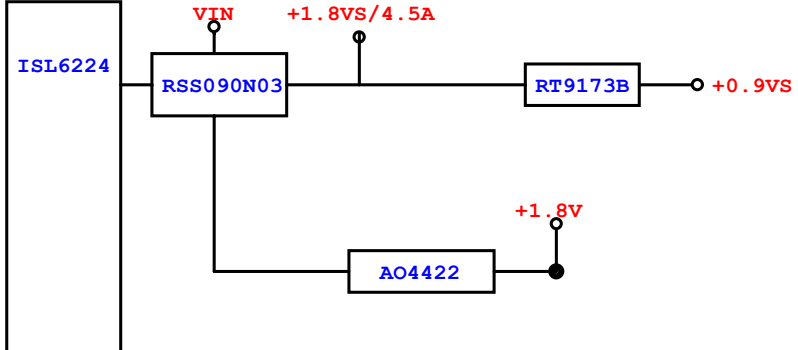
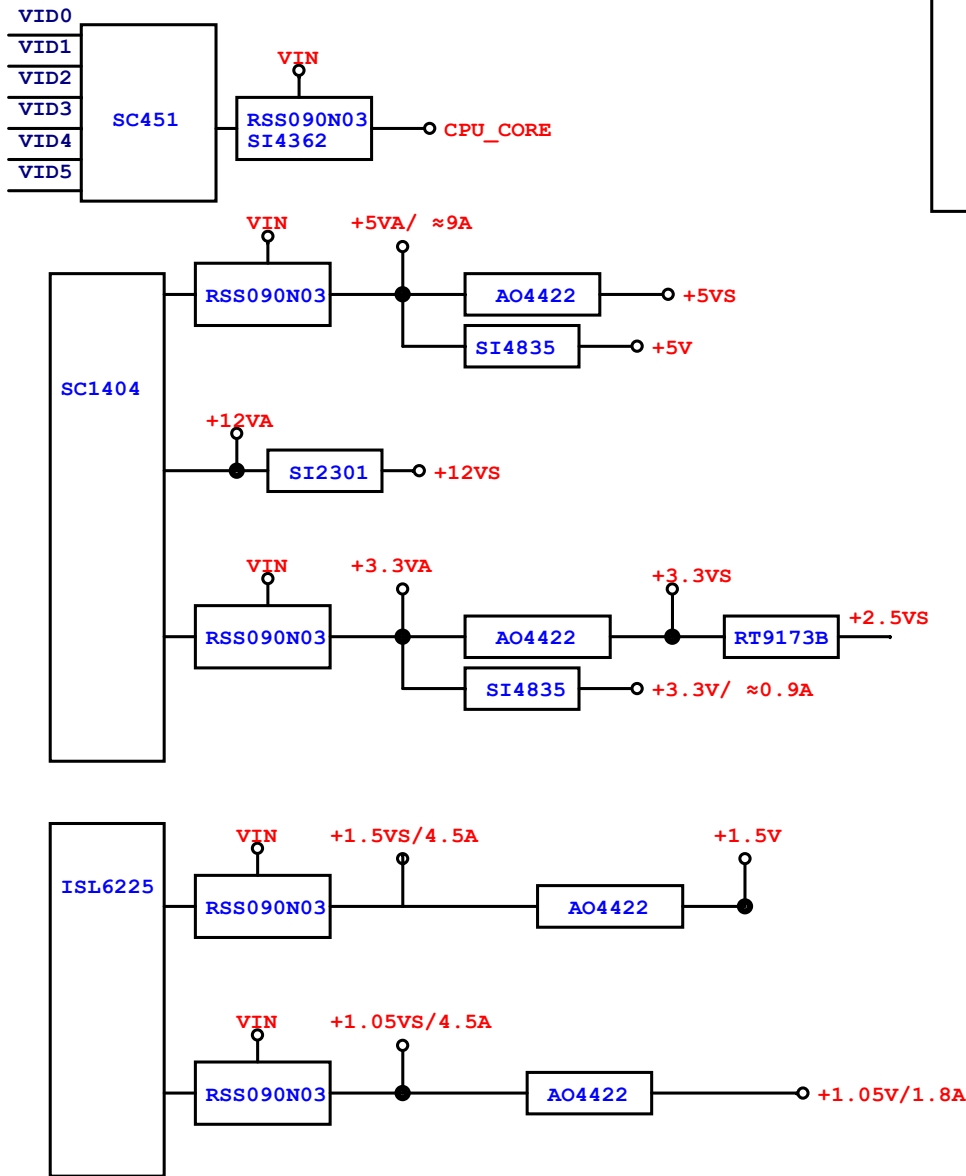
PG21 LANRTL8100CL
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PG24 EC IT8510E / BIOS / Keyboard & TP CONN
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PG27 +3.3V / +5V / +12V
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UNIWILL COMPUTER CORP.			
Title		M50EA0	
Size	Document Number	INDEX	
Custom	3145	Rev B	
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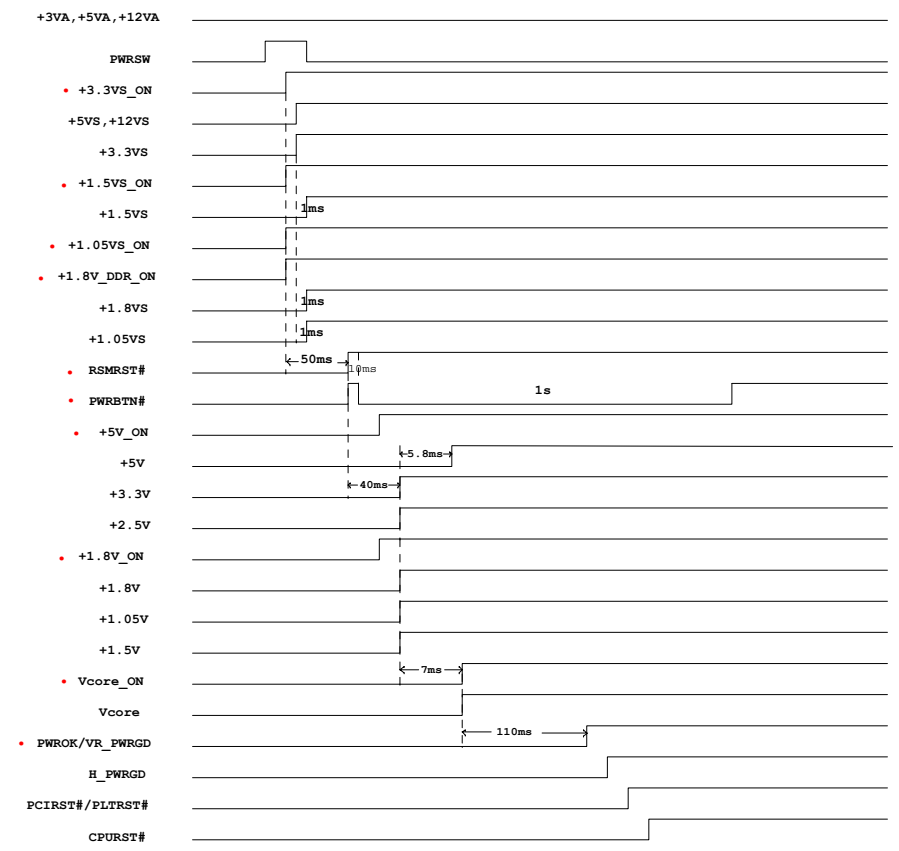
M50EA0 BLOCK DIAGRAM



POWER BLOCK DIAGRAM



POWER Sequence



ICH6-M GPIO	
GPI6	BM_BUSY#
GP7	
GP8	EC_EXTSMI#
GPI11	SMB_ALERT#
GPI12	
GPI13	
GPO18	PM_STPPCI_ICH#
GPO19	
GPO20	PM_STPCPU_ICH#
GPO21	TPM_EN
GPO23	
GPI024	
GPI025	
GPI026	SATA0_GP
GPI027	
GPI028	
GPI029	PNLSW1
GPI030	PNLSW2
GPI031	PNLSW0
GPI032	PM_CLKRUN#
GPI033	
GPI034	

ITE8510E GPIO	
GPCF0	TURBO#/PHOTO
GPCF1	SILENT#/TV
GPCF2	BAT_SEL
GPCF3	BAT_THROT_EN
GPCF4	TP_CLK
GPCF5	TP_DATA
GPCF6	MAIL#/DVD
GPCF7	BROWSER#/MP3
GPI0	SCROLL#
GPI1	CAPS#
GPI2	NUM#
GPI3	CHGLED_ON#
GPI4	A/W_LED1#
GPI5	SUSLED_ON#
GPI6	A/W_LED2#
GPH0	+1.8V_DDR_ON
GPH1	+1.8V_ON
GPH2	+1.05VS_ON
GPH3	+3.3VS_ON
GPH4	+5V_ON
GPH5	SET_V
GPH6	+1.5VS_ON
GPH7	VCORE_ON
GPG4	
GPG5	LCDSW
GPG6	MUTE#
GPG7	EXTTS#0
GPB0	CELERON_VO_DET
GPB1	TURBO_LED#
GPB2	PM_RSMRST#
GPB3	BAT_SMBCLK
GPB4	BAT_SMBDAT
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	RFLED_ON#
GPE0	
GPE1	CPU_BSEL0
GPE2	TP_BTU
GPE3	TP_BTD
GPE4	PWRSW
GPE5	LID#
GPE6	RF_OFF
GPE7	PM_SLP_S3#
GPD0	ADAP_IN
GPD1	AW#/CD
GPD2	PCI_RST#/PLT_RST#
GPD3	EC_EXTSMI#
GPD4	
GPD5	
GPD6	CLKREQ#
GPD7	EC_PREST#
GPA0	BTL_BEEP
GPA1	EC_VID1
GPA2	EC_VID2
GPA3	EC_VID3
GPA4	EC_VID4
GPA5	SMP1_EN#
GPA6	SMP2_EN#
GPA7	PWRBTN#

ITE8510E GPIO	
GPC0	PWROK
GPC1	BAT2_SMBCLK
GPC2	BAT2_SMBDAT
GPC3	
GPC4	
GPC5	A/W_LED3#
GPC6	CHG_ON
GPC7	SILENT_LED#
ANOTE	
CATHODE	

SB INT_PIRQ List	
INT_PIRQA	CARD BUS
INT_PIRQB	Mini PCI
INT_PIRQC	1394
INT_PIRQD	LAN
INT_PIRQE	CARD BUS(op)
INT_PIRQF	Mini PCI
INT_PIRQG	NC
INT_PIRQH	NC

CPU				
	CPU CORE(V)	ICC(mA)	W	TEMP()
2.0G	1.525	35.7	54.3	69
2.2G	1.525	37.5	57.1	70
2.26G	1.525	38.1	58.0	70
2.4G	1.525	39.3	59.8	71
2.5G	1.525	40	61.0	72
2.53G	1.525	40.4	61.5	72
2.6G	1.525	41.05	62.6	72
2.66G	1.525	43.35	66.1	74
2.8G	1.525	44.86	68.4	75
3.06G	1.525	55.9	85.2	81

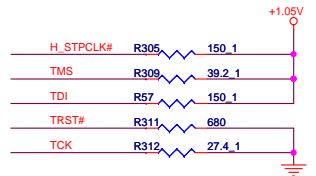
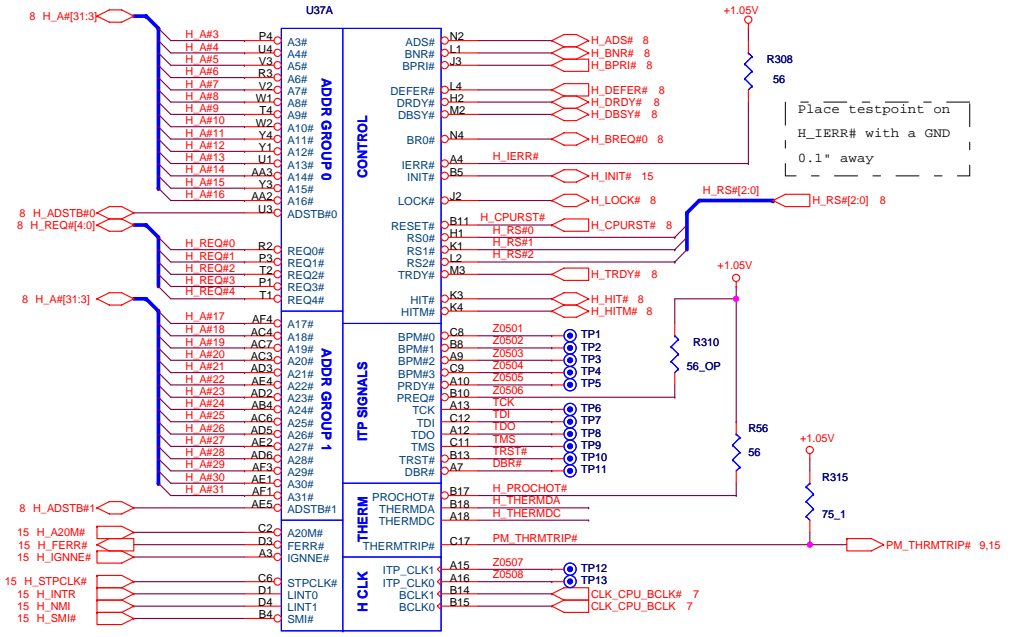
MCHE			
VCC	ICC(mA)	W	TEMP()
+3.3V	108.19	0.357	70
+3.3VA	501.3	1.254	
+2.5V	1390	2.502	
+1.5V	33.4	0.084	
+VCCP	10	0.018	
+VCC_GMCH_CORE	266	0.452	

ICH6-M			
VCC	ICC(mA)	W	TEMP()
+3.3V	96	0.315	70
+3.3VA	275	0.909	
+1.5V	487	0.876	
+1.5VA	27	0.049	
+3.3VA_RTC	0.003	0.00001	

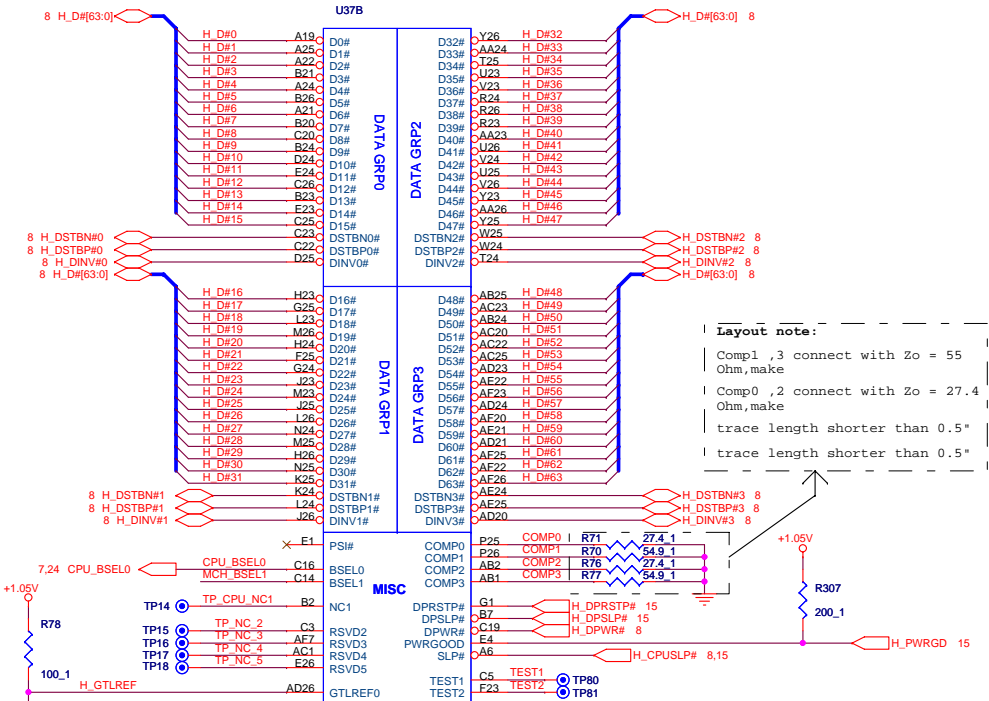
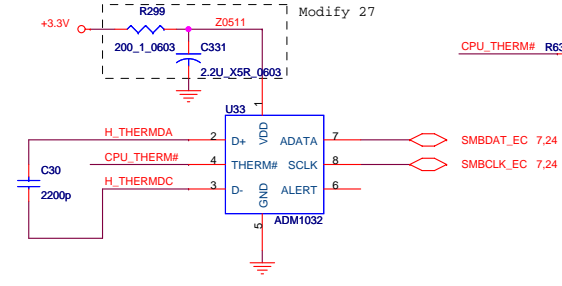
ITE8510E			
VCC	ICC(mA)	W	TEMP()
+3.3V	300	1	70

CLOCK GENERATOR			
VCC	ICC(mA)	W	TEMP()
+3.3V	180	0.594	70

ADM1032			
VCC	ICC	W	TEMP()
+3.3V	170uA	0.56mW	150



CPU Thermal Sensor



Layout note: 0.5" max length.

Layout note:
Comp1,3 connect with Zo = 55 Ohm,make
Comp0,2 connect with Zo = 27.4 Ohm,make
trace length shorter than 0.5"
trace length shorter than 0.5"

	BSEL0	BSEL1
PSB400	1	0
PSB533(default)	0	0

ICS954206 BSEL Settings:
01=PSB400(BSEL0=1 BSEL1=0)
00=PSB533(BSEL1=0 BSEL0=0)

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TitleM50EA0

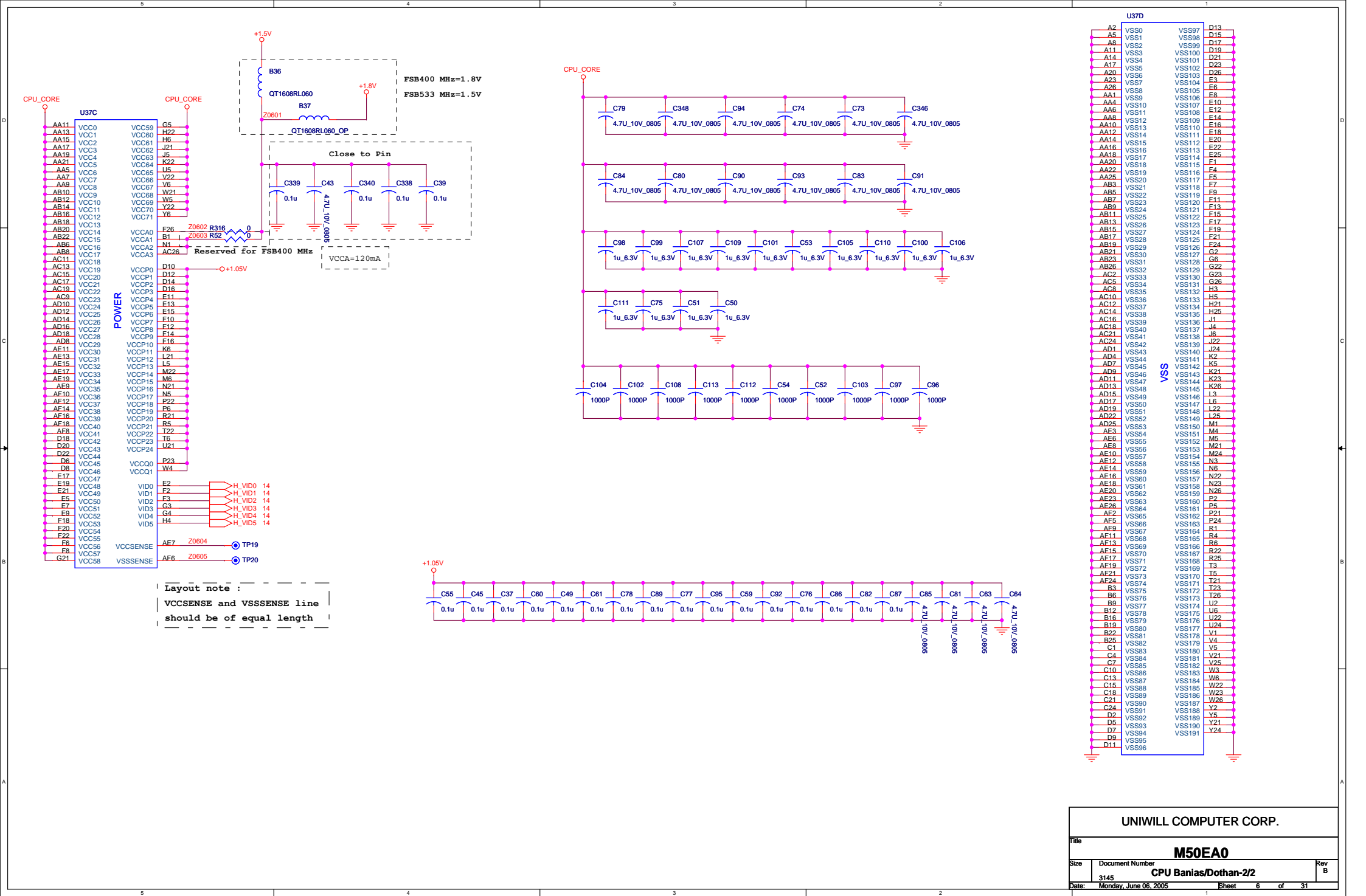
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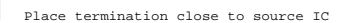
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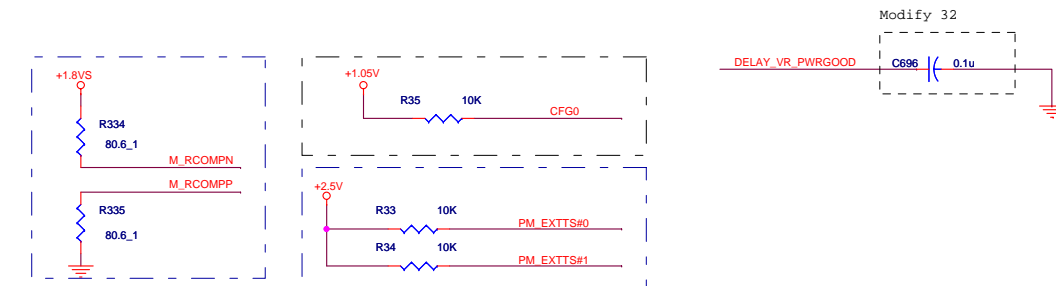
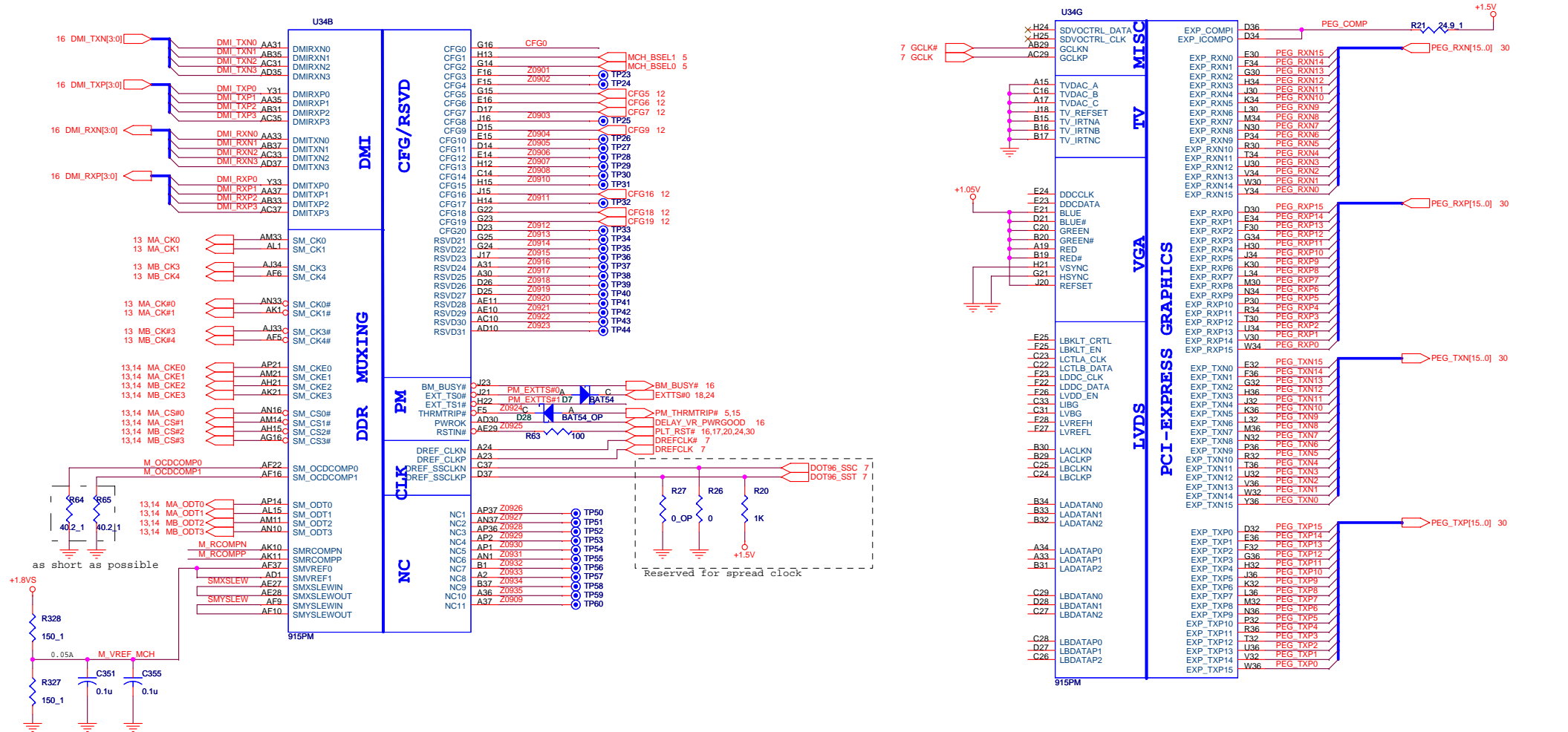
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CFG0	CFG1	CFG2	Host Clock frequency
1	0	1	100
1	0	0	133

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NB DDRCLK_VGA_PCIEXPR-2/5

13 MA_DQ[63:0]

MA_DQ0 AG35 SADO0
MA_DQ1 AH36 SADO1
MA_DQ2 AL37 SADO2
MA_DQ3 AL37 SADO3
MA_DQ4 AH36 SADO4
MA_DQ5 AJ35 SADO5
MA_DQ6 AK37 SADO6
MA_DQ7 AL34 SADO7
MA_DQ8 AM36 SADO8
MA_DQ9 AN35 SADO9
MA_DQ10 AP32 SADO10
MA_DQ11 AM31 SADO11
MA_DQ12 AM34 SADO12
MA_DQ13 AM35 SADO13
MA_DQ14 AL32 SADO14
MA_DQ15 AM32 SADO15
MA_DQ16 AN31 SADO16
MA_DQ17 AP31 SADO17
MA_DQ18 AN28 SADO18
MA_DQ19 AP28 SADO19
MA_DQ20 AL30 SADO20
MA_DQ21 AM30 SADO21
MA_DQ22 AM28 SADO22
MA_DQ23 AL28 SADO23
MA_DQ24 AP27 SADO24
MA_DQ25 AM27 SADO25
MA_DQ26 AM23 SADO26
MA_DQ27 AM22 SADO27
MA_DQ28 AL23 SADO28
MA_DQ29 AM24 SADO29
MA_DQ30 AN22 SADO30
MA_DQ31 AP22 SADO31
MA_DQ32 AM8 SADO32
MA_DQ33 AL8 SADO33
MA_DQ34 AP7 SADO34
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MA_DQ36 AP11 SADO36
MA_DQ37 AL10 SADO37
MA_DQ38 AL7 SADO38
MA_DQ39 AM7 SADO39
MA_DQ40 AN5 SADO40
MA_DQ41 AN8 SADO41
MA_DQ42 AN3 SADO42
MA_DQ43 AP3 SADO43
MA_DQ44 AP6 SADO44
MA_DQ45 AM6 SADO45
MA_DQ46 AM3 SADO46
MA_DQ47 AK2 SADO47
MA_DQ48 AK2 SADO48
MA_DQ49 AK3 SADO49
MA_DQ50 AG2 SADO50
MA_DQ51 AG1 SADO51
MA_DQ52 AL3 SADO52
MA_DQ53 AM2 SADO53
MA_DQ54 AH3 SADO54
MA_DQ55 AG3 SADO55
MA_DQ56 AE3 SADO56
MA_DQ57 AE3 SADO57
MA_DQ58 AD6 SADO58
MA_DQ59 AC4 SADO59
MA_DQ60 AE2 SADO60
MA_DQ61 AF1 SADO61
MA_DQ62 AD4 SADO62
MA_DQ63 AD5 SADO63

U34C

DDR SYSTEM MEMORY A

915PM

SA_BS0#
SA_BS1#
SA_BS2#

AK15 MA_BA0
AK16 MA_BA1
AL21 MA_BA2
AJ37 MA_DM0
AP35 MA_DM1
AL29 MA_DM2
AP24 MA_DM3
AP9 MA_DM4
AP4 MA_DM5
AJ2 MA_DM6
AD3 MA_DM7

MA_BA[2:0] 13,14

MA_DM[7:0] 13

AK36 MA_DQS0
AP33 MA_DQS1
AN23 MA_DQS2
AP23 MA_DQS3
AM8 MA_DQS4
AM4 MA_DQS5
AJ1 MA_DQS6
AE5 MA_DQS7

MA_DQS[7:0] 13

AK35 MA_DQS#0
AP34 MA_DQS#1
AN30 MA_DQS#2
AN23 MA_DQS#3
AN8 MA_DQS#4
AM5 MA_DQS#5
AH1 MA_DQS#6
AE4 MA_DQS#7

MA_DQS#7[0] 13

AL17 MAA_A0
AP17 MAA_A1
AP18 MAA_A2
AM17 MAA_A3
AN18 MAA_A4
AM18 MAA_A5
AL19 MAA_A6
AP20 MAA_A7
AM19 MAA_A8
AL20 MAA_A9
AM16 MAA_A10
AM20 MAA_A11
AM15 MAA_A12
AM15 MAA_A13

MAA_A[13:0] 13,14

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MA_RAS# 13,14

MA_WE# 13,14

MA_WE# 13,14

13 MB_DQ[63:0]

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MB_DQ1 MA1 SBDQ1
MB_DQ2 AG32 SBDQ2
MB_DQ3 AG36 SBDQ3
MB_DQ4 AE34 SBDQ4
MB_DQ5 AE33 SBDQ5
MB_DQ6 AE30 SBDQ6
MB_DQ7 AE31 SBDQ7
MB_DQ8 AH33 SBDQ8
MB_DQ9 AH32 SBDQ9
MB_DQ10 AK31 SBDQ10
MB_DQ11 AG30 SBDQ11
MB_DQ12 AG34 SBDQ12
MB_DQ13 AG33 SBDQ13
MB_DQ14 AH31 SBDQ14
MB_DQ15 AJ31 SBDQ15
MB_DQ16 AK30 SBDQ16
MB_DQ17 AJ30 SBDQ17
MB_DQ18 AH29 SBDQ18
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MB_DQ60 AC8 SBDQ60
MB_DQ61 AC7 SBDQ61
MB_DQ62 AA4 SBDQ62
MB_DQ63 AA5 SBDQ63

U34D

DDR SYSTEM MEMORY B

915PM

SB_BS0#
SB_BS1#
SB_BS2#

AJ15 MB_BA0
AG17 MB_BA1
AG21 MB_BA2

MB_BA[2:0] 13,14

AF32 MB_DM0
AK34 MB_DM1
AK27 MB_DM2
AK24 MB_DM3
AJ10 MB_DM4
AE7 MB_DM5
AB7 MB_DM6
AB7 MB_DM7

MB_DM[7:0] 13

AF34 MB_DQS0
AK32 MB_DQS1
AJ28 MB_DQS2
AK23 MB_DQS3
AM10 MB_DQS4
AH6 MB_DQS5
AF9 MB_DQS6
AB4 MB_DQS7

MB_DQS[7:0] 13

AF35 MB_DQS#0
AK33 MB_DQS#1
AK28 MB_DQS#2
AJ23 MB_DQS#3
AL10 MB_DQS#4
AH7 MB_DQS#5
AF7 MB_DQS#6
AB5 MB_DQS#7

MB_DQS#7[0] 13

AH17 MBA_A0
AK17 MBA_A1
AH18 MBA_A2
AJ18 MBA_A3
AK18 MBA_A4
AJ19 MBA_A5
AK19 MBA_A6
AH19 MBA_A7
AJ20 MBA_A8
AH20 MBA_A9
AJ16 MBA_A10
AG18 MBA_A11
AG20 MBA_A12
AG15 MBA_A13

MBA_A[13:0] 13,14

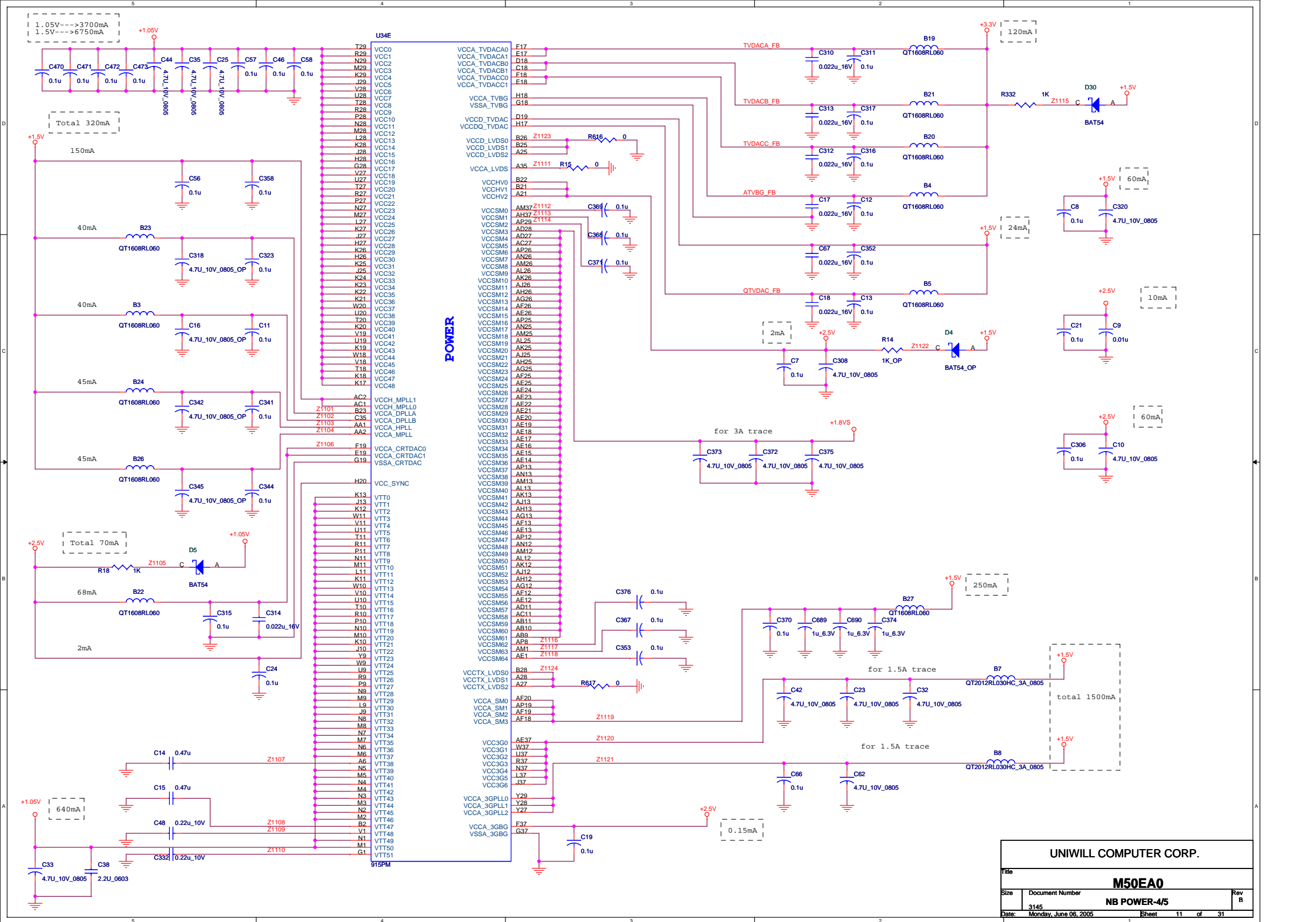
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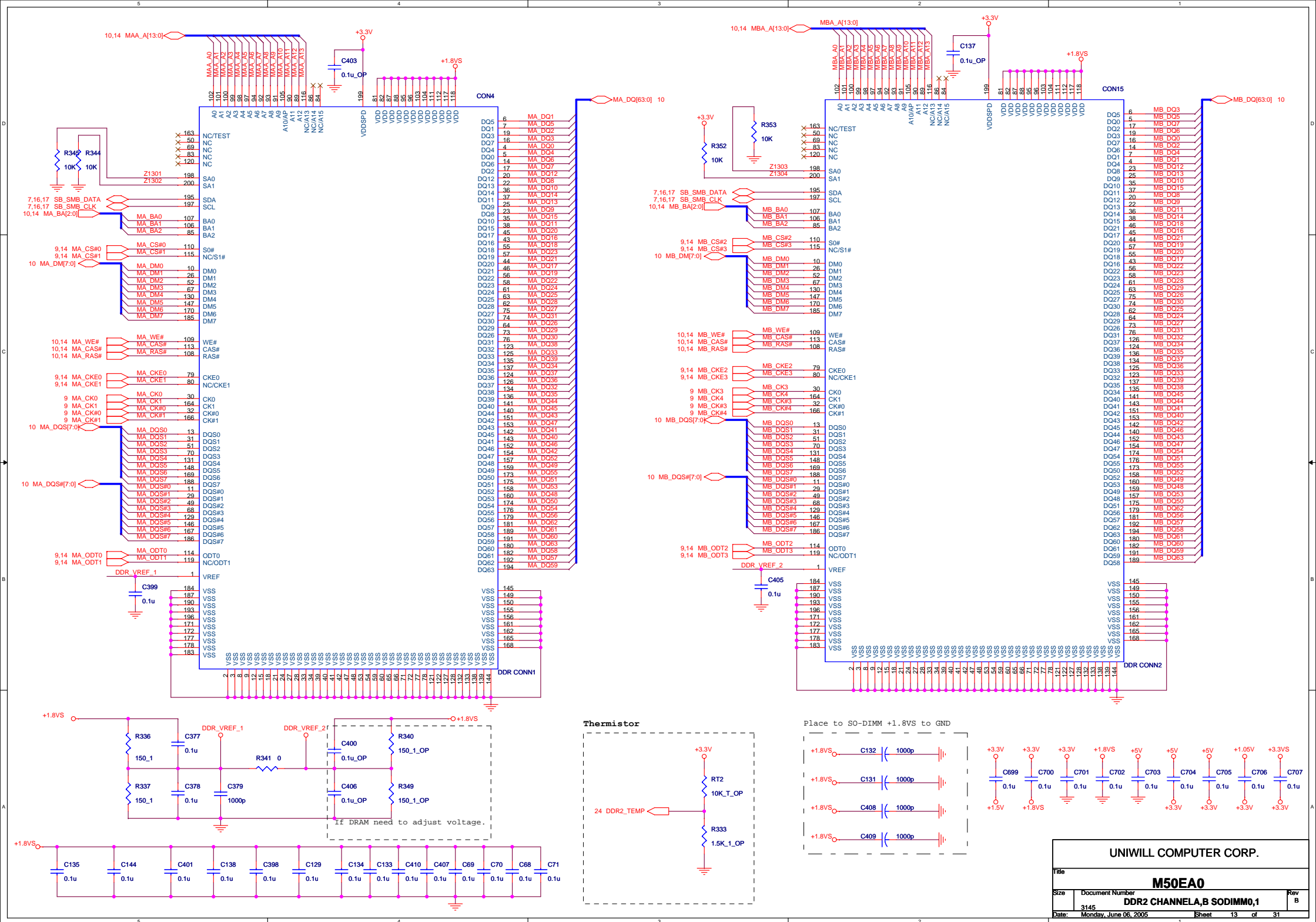
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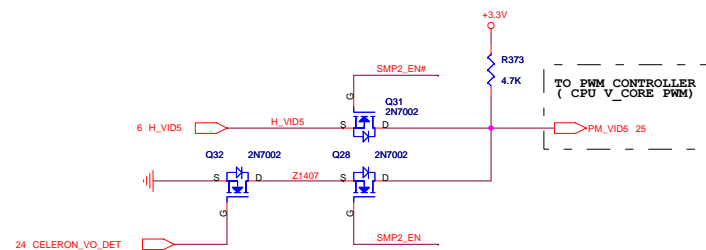
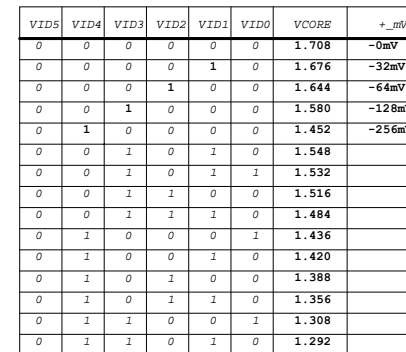
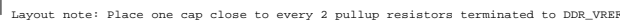
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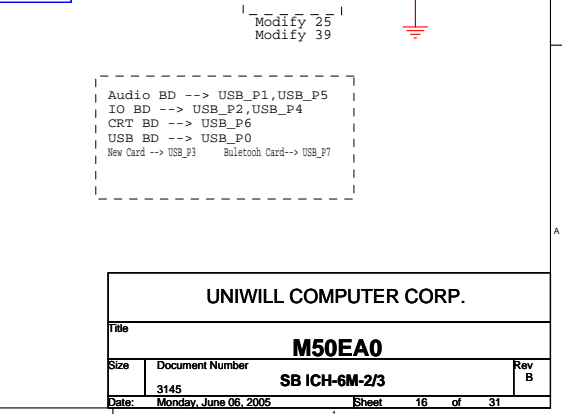
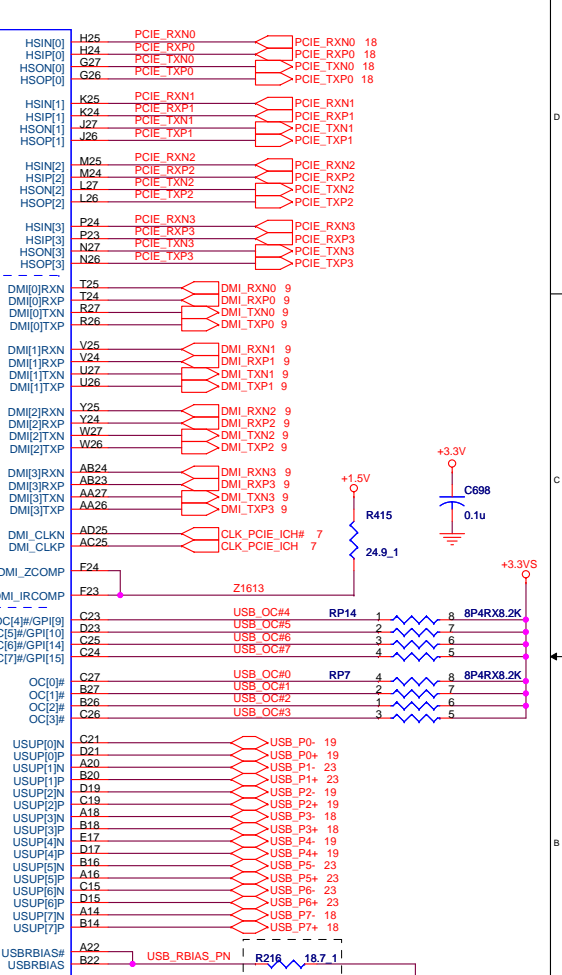
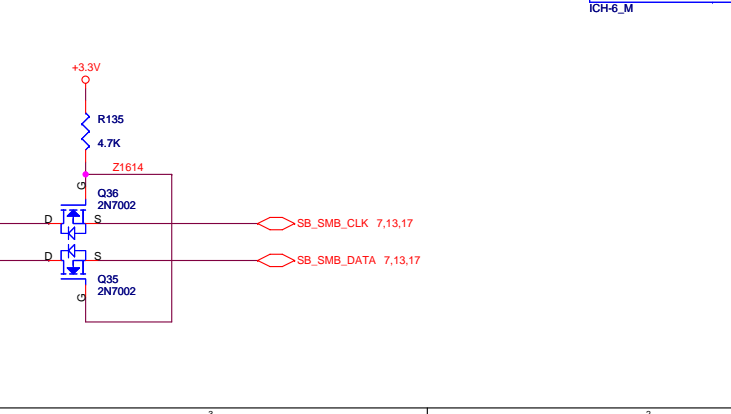
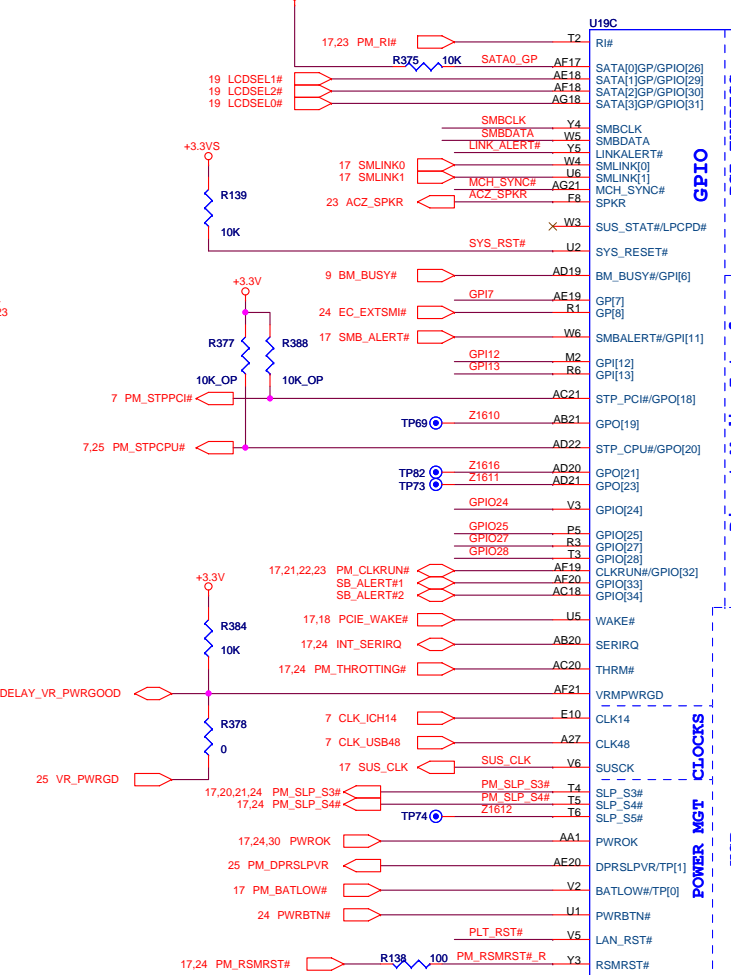
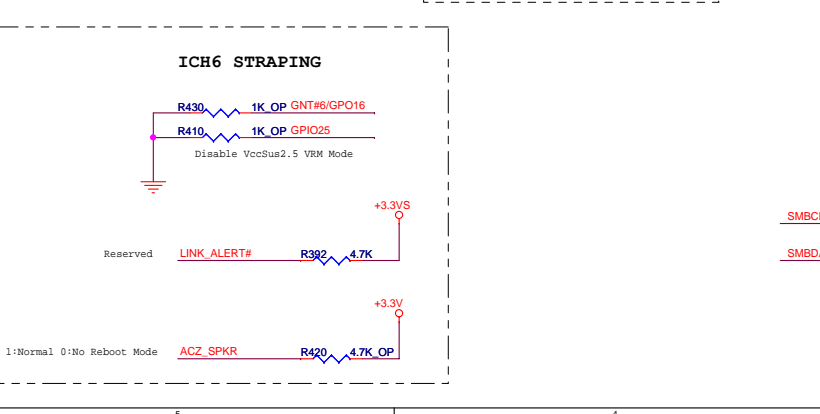
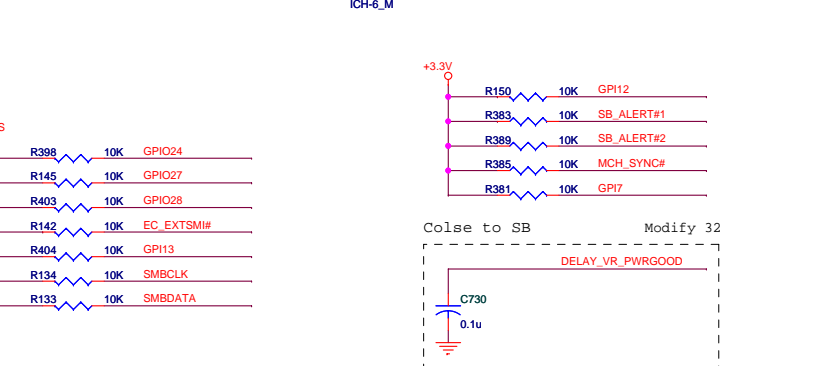
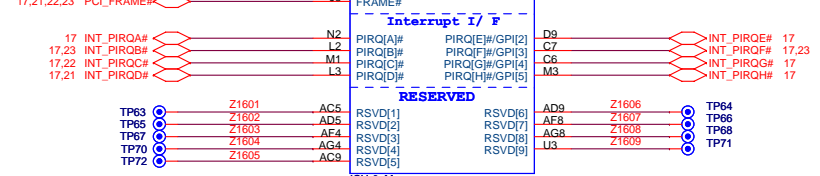
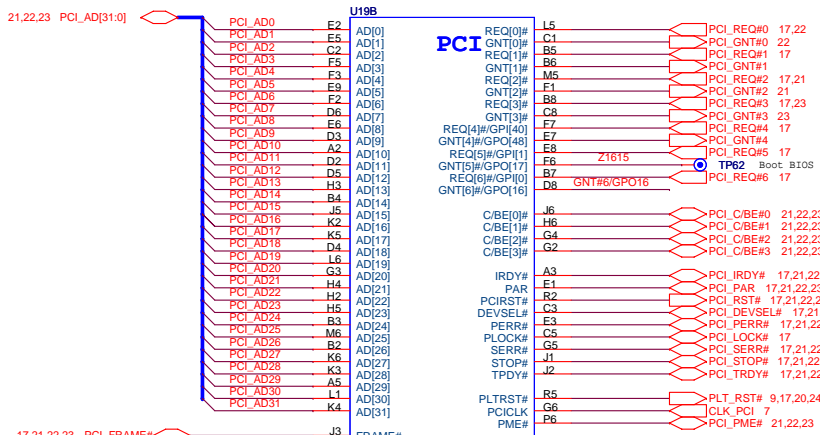
UNIWill COMPUTER CORP.

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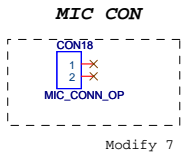




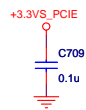
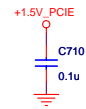
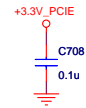
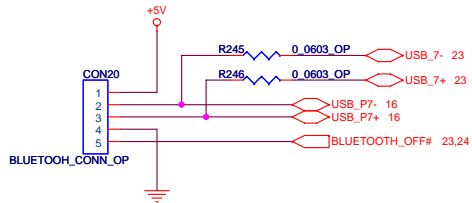




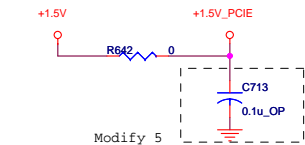
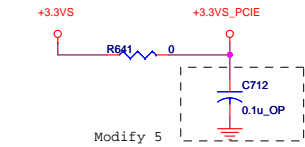
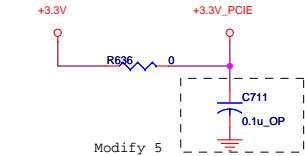
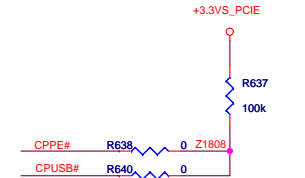
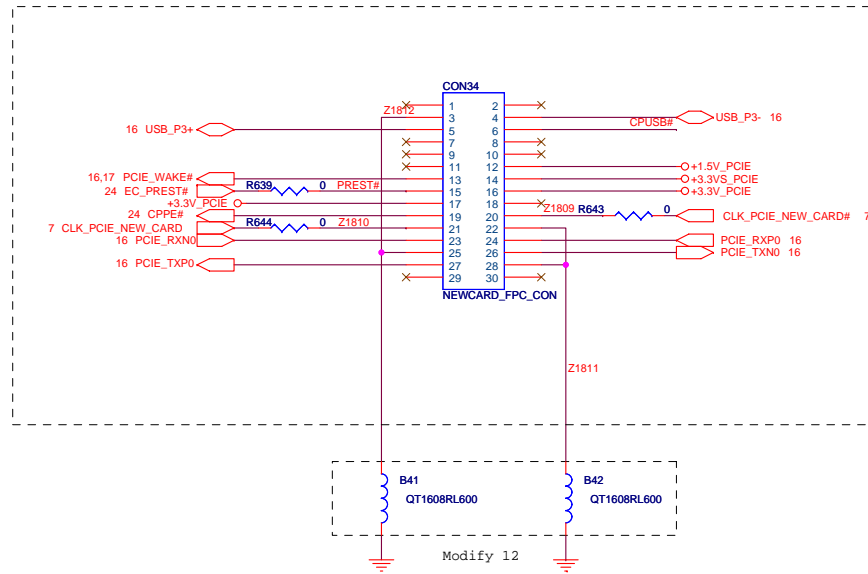
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IO BD --> USB_P2, USB_P4
CRT BD --> USB_P6
USB BD --> USB_P0
New Card --> USB_P3 Bluetooth Card --> USB_P7



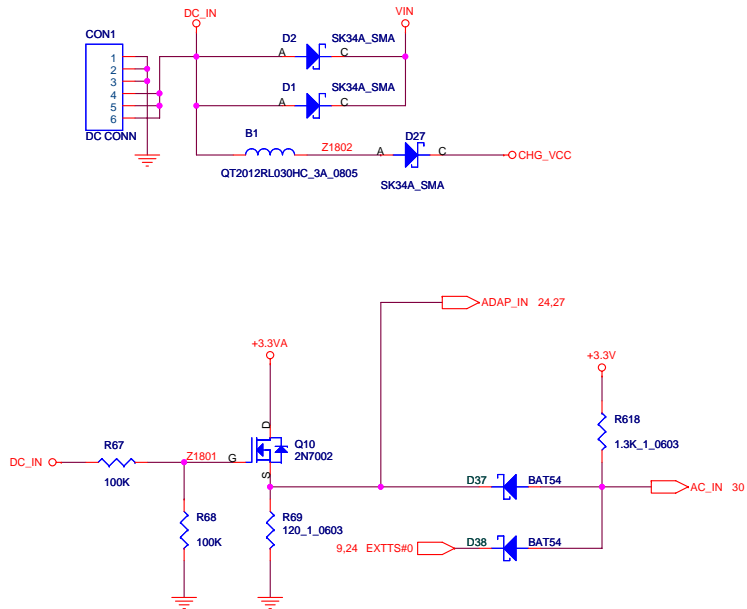
BLUETOOTH CONN



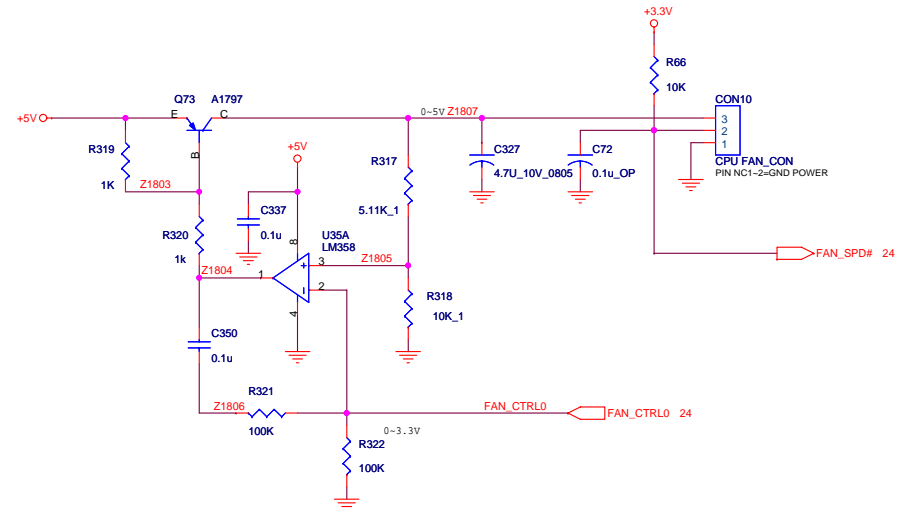
Modify 16



DC IN

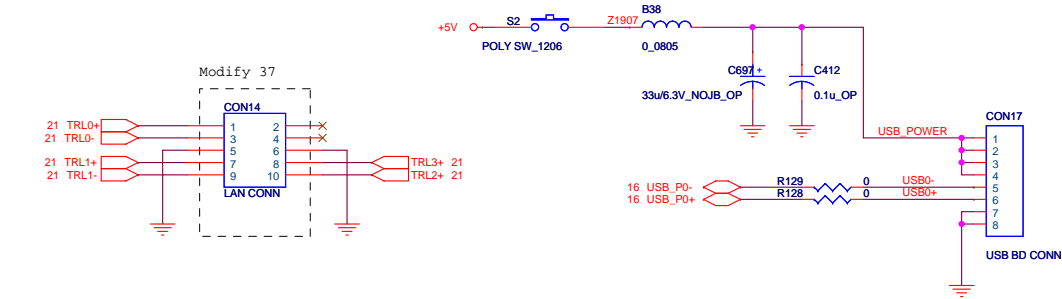
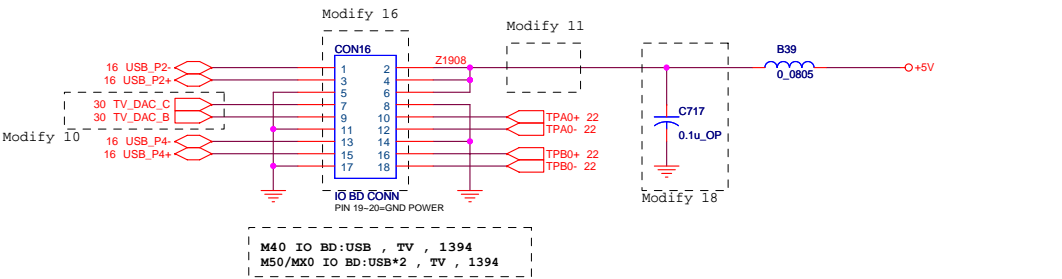


CPU FAN CONTROL

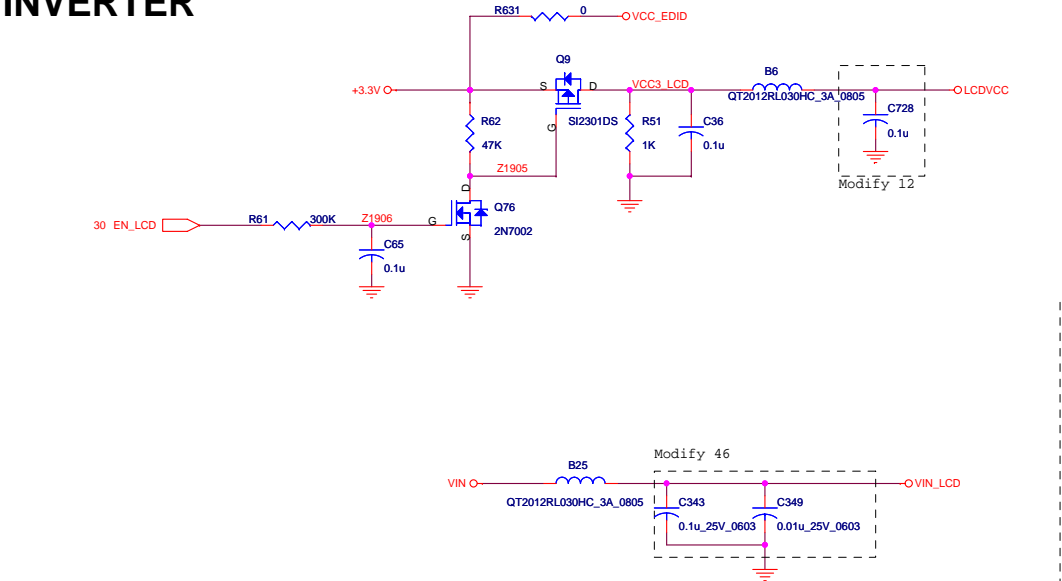


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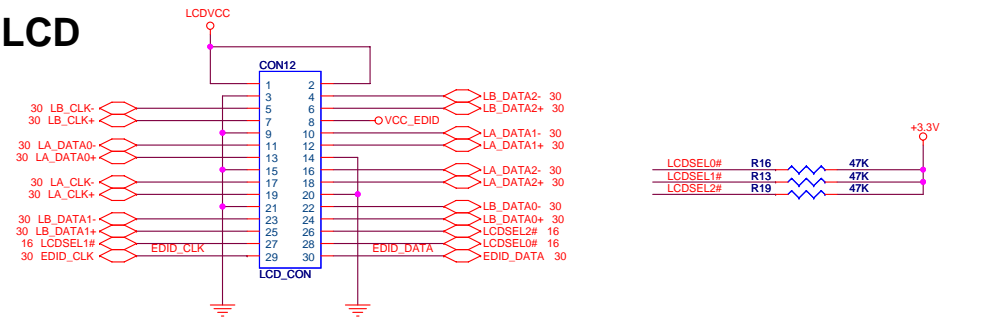
Title			M50EA0		
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INVERTER

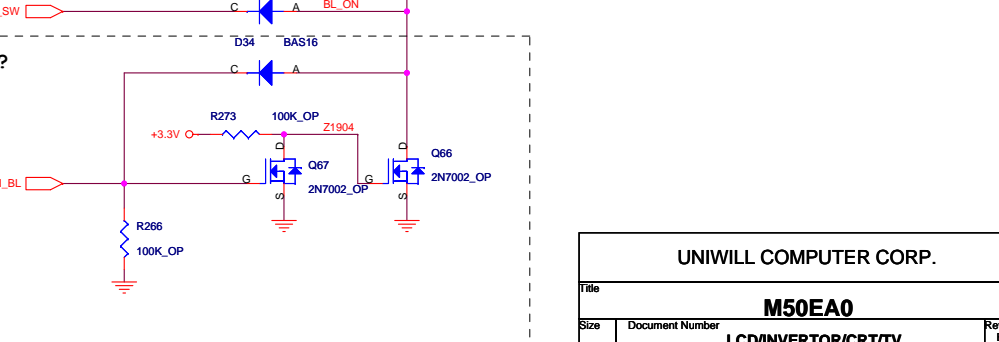
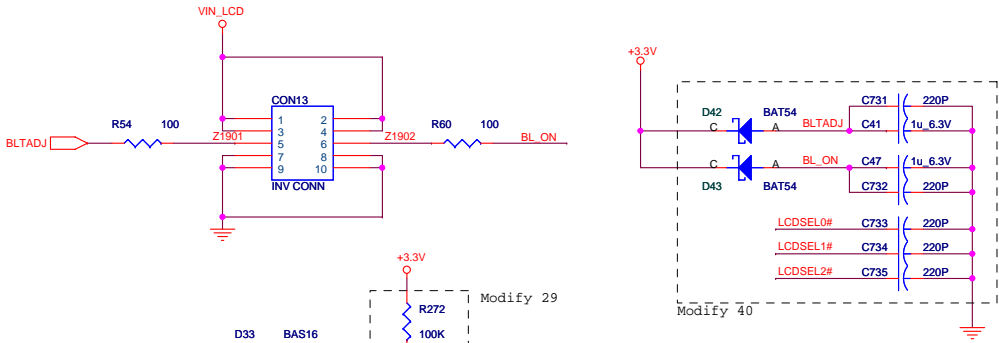


LCD



PANNEL SELECT

LCDSEL2#	LCDSEL1#	LCDSEL0#	
L	L	L	1024X768
L	L	H	1400X1050
L	H	L	1280X800
L	H	H	reserved
H	L	L	reserved
H	L	H	1680X1050
H	H	L	1920X1200
H	H	H	1440X900

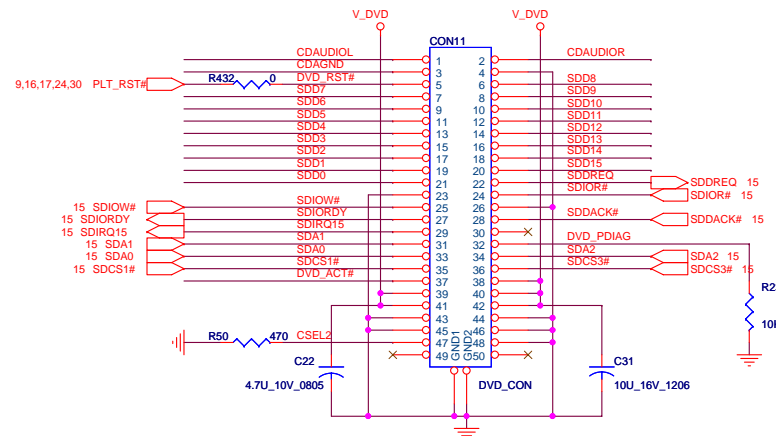
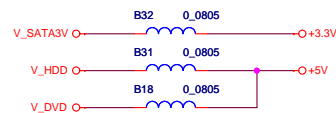
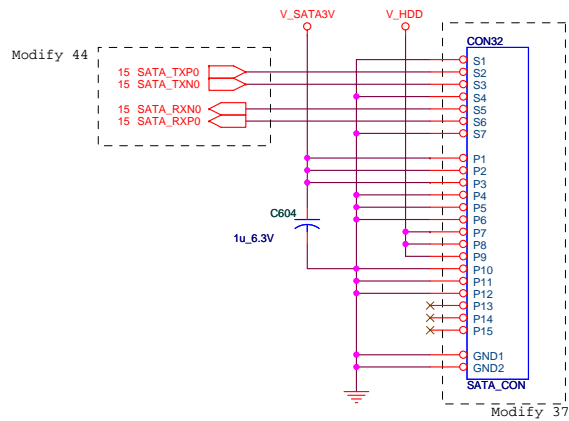


UNIWILL COMPUTER CORP.

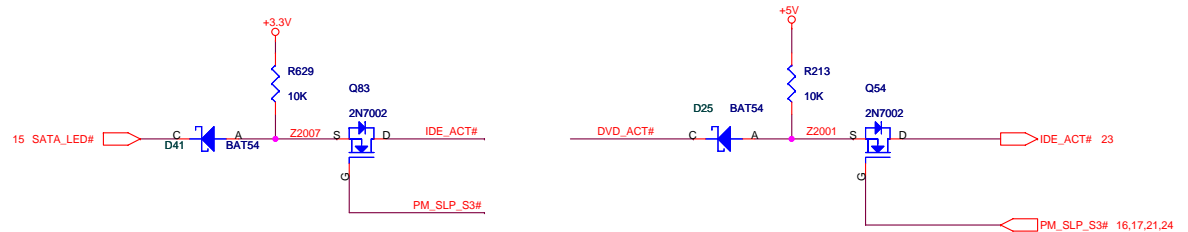
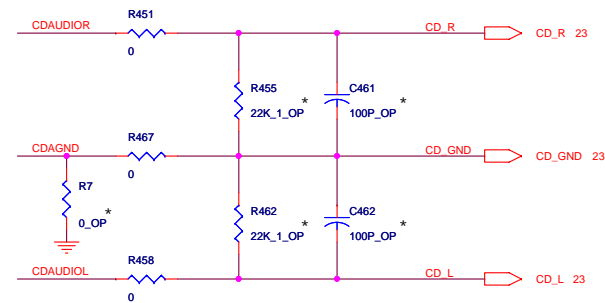
M50EA0

Size Document Number
3145 LCD/INVERTOR/CRT/TV

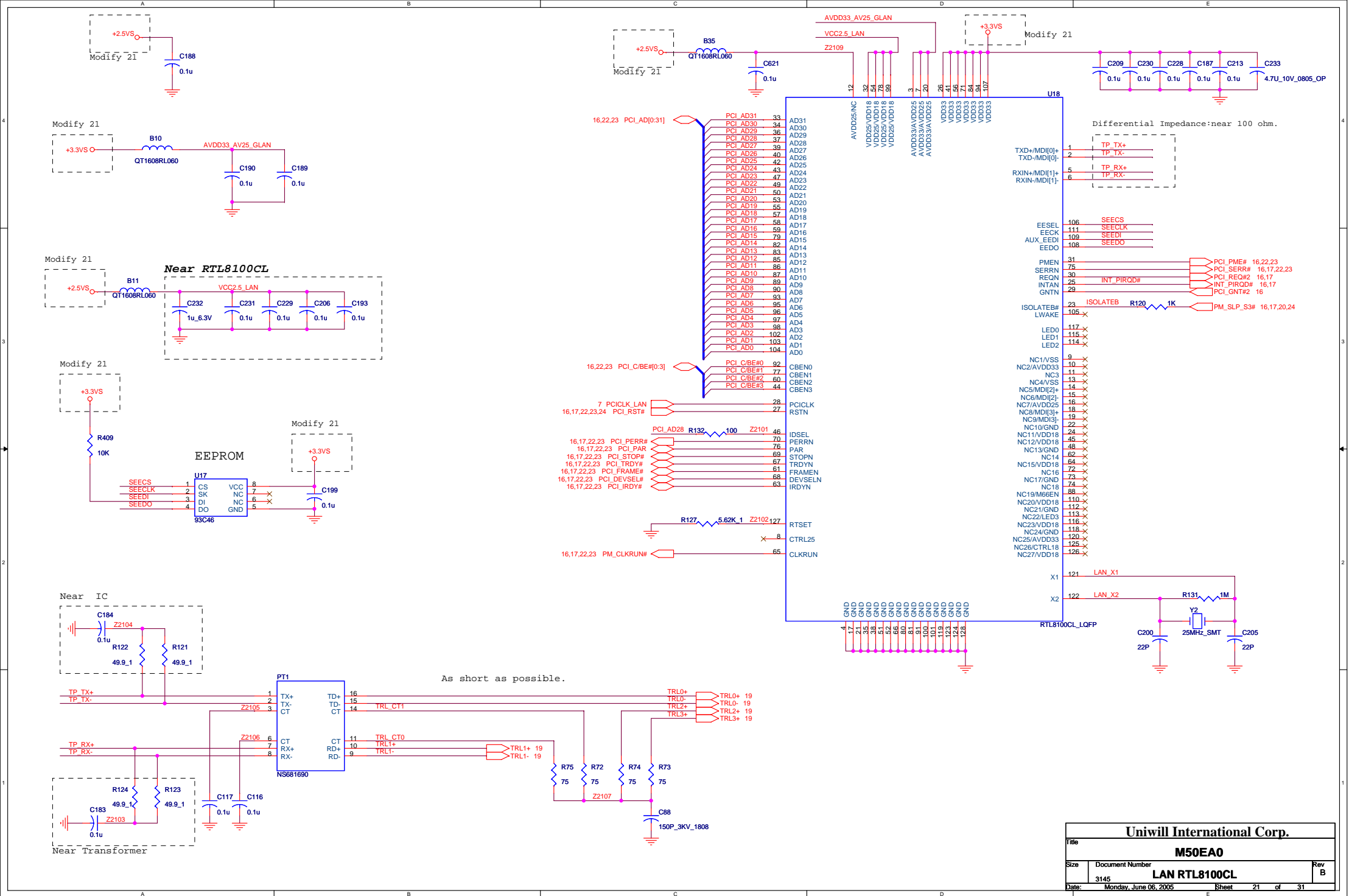
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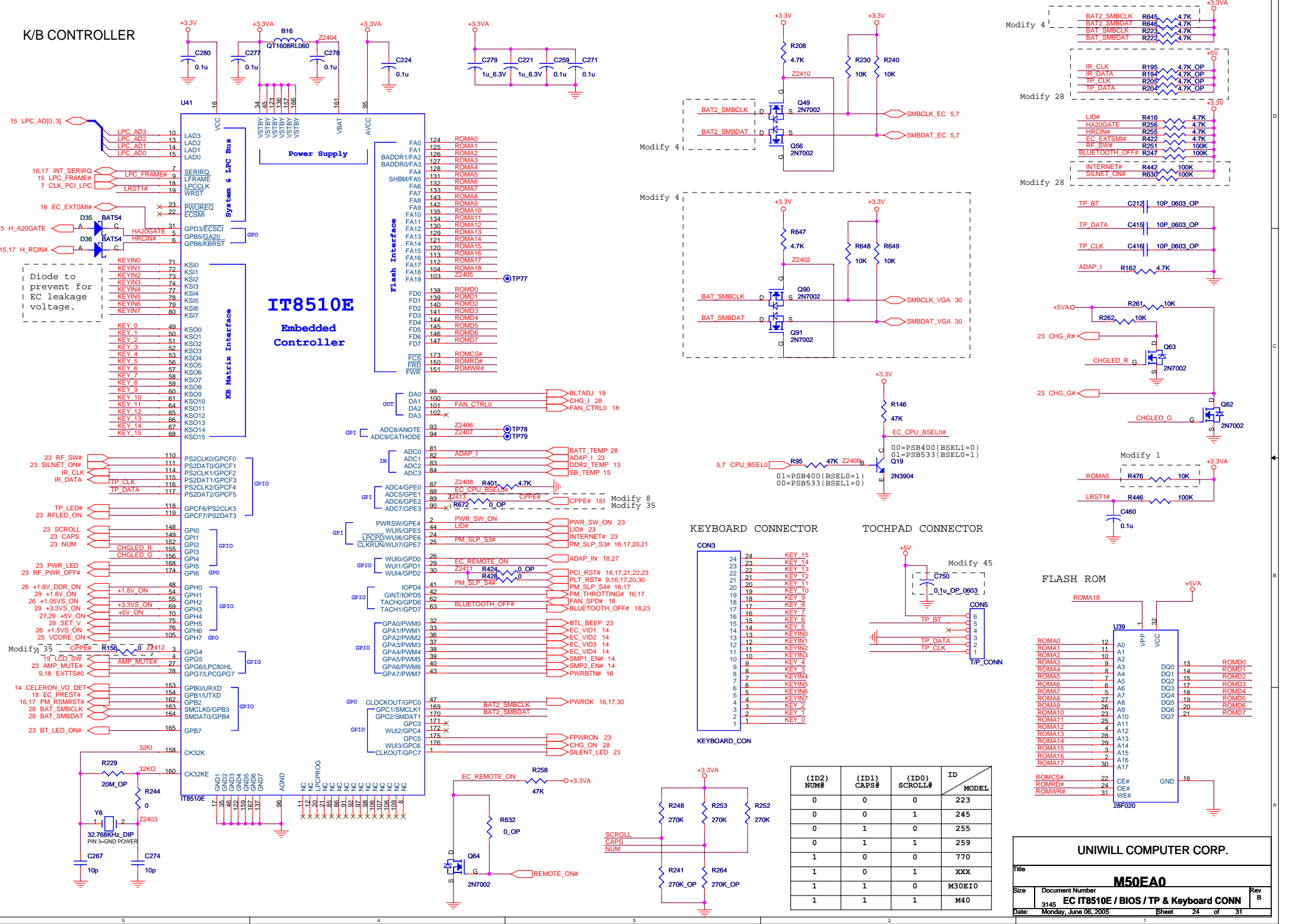
SDD[0..15] 15



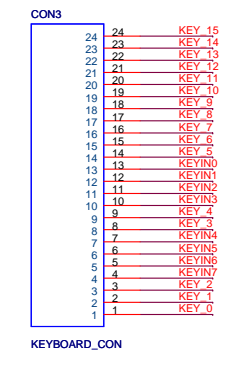
UNIWILL COMPUTER CORP.			
Title		M50EA0	
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	3145	SATA HDD/CD-ROM	
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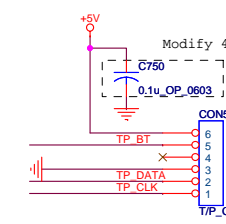
K/B CONTROLLER



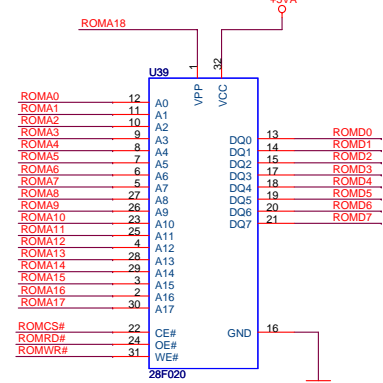
KEYBOARD CONNECTOR



TOCHPAD CONNECTOR



FLASH ROM



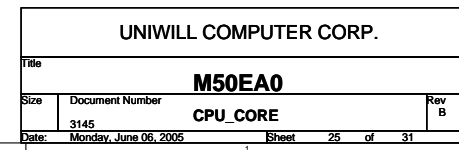
UNIWill COMPUTER CORP.

Title: **M50EA0**

Size: 3145 Document Number: **EC IT8510E / BIOS / TP & Keyboard CONN** Rev B

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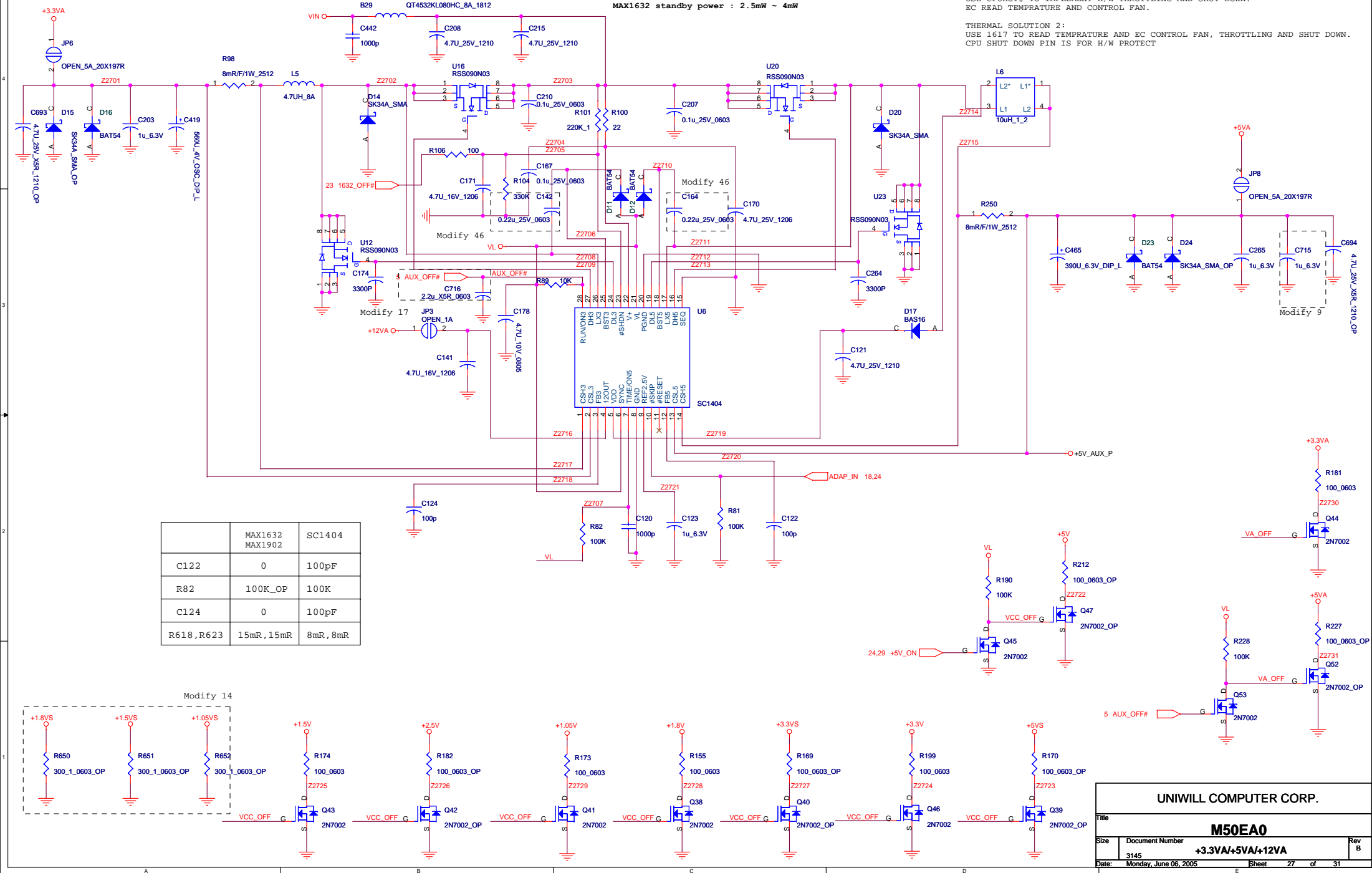
(ID2) NUM#	(ID1) CAPS#	(ID0) SCROLL#	ID	MODEL
0	0	0	223	
0	0	1	245	
0	1	0	255	
0	1	1	259	
1	0	0	770	
1	0	1	XXX	
1	1	0	M30E10	
1	1	1	M40	



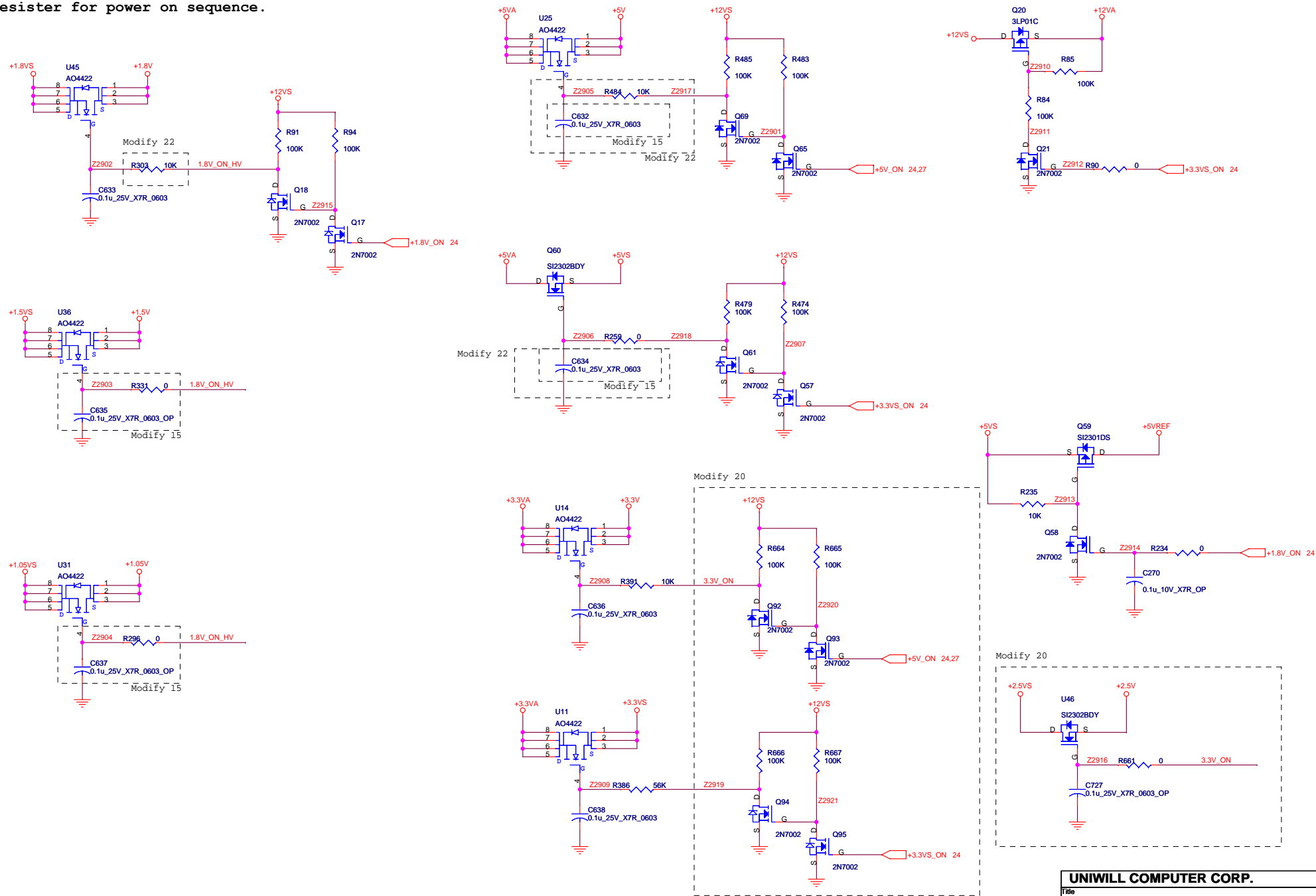
MAX1632 shutdown current : 4~10uA (SHDN# pin = low)
MAX1632 standby power : 2.5mW ~ 4mW

THERMAL SOLUTION 1:
USE CPUHOT# TO IMPLEMENT H/W THROTTLING AND SHUT DOWN.
EC READ TEMPERATURE AND CONTROL FAN.

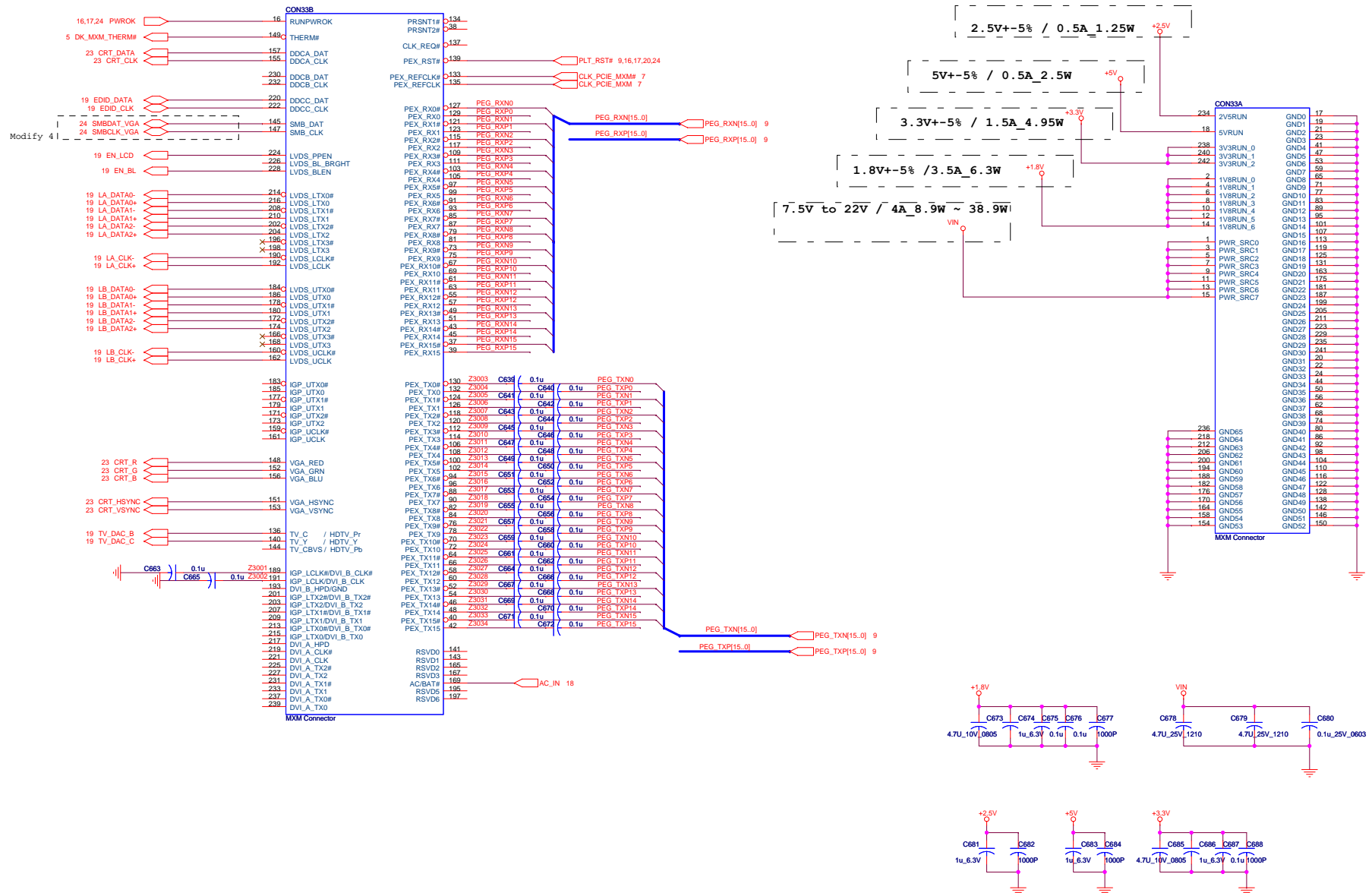
THERMAL SOLUTION 2:
USE 1617 TO READ TEMPERATURE AND EC CONTROL FAN, THROTTLING AND SHUT DOWN.
CPU SHUT DOWN PIN IS FOR H/W PROTECT



@Modify resistor for power on sequence.



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R:A to R:B Change Note

Modify 1: R476 from 4.7K to 10K for current leakage
Modify 2: Change C362 from 22p_OP to 68p for +1.5V reliability
Modify 3: Change R330 from 1.05K_1 to 2K_1 for OCP function
Modify 4: Modify EC SM_BUS pin define and add VGA SM_BUS circuit
Modify 5: Change CON2 (S/W CONN) Pin 20,21,31,32 define and Add C714,R668,669,670 , reserve C711,712,713(0.1u_OP) for EMI
Modify 6: Change CON6 (Audio CONN) Pin define
Modify 7: CON18 MIC_CONN_OP
Modify 8: Change EC Pin 63,154,89,172,118 define and R225 from 47K to 0 ohm
Modify 9: Add C715 for +5VA ripple
Modify 10: Change CON16 TV-DAC (Pin 7,9) define for MX0EIO
Modify 11: Remove S3 (Poly switch)
Modify 12: Add B41,B42,C728 for EMI and Change CON34 Footprint for ME issue
Modify 13: Modify Y4 BOM P/N from 25G143186-30 to 25G143186-31
Modify 14: Add R650_OP,R651_OP,R652_OP circuit
Modify 15: Modify R331,R296 from 22K to 0 ohm and C632,C634,C635,C637 _OP for power sequence
Modify 16: Change CON16,CON34 Footprint and BOM P/N
Modify 17: Add C716 for EC +3.3VA reset fail issue
Modify 18: Add R653,654,656,657,658,659,660 (0 ohm) and reserve C720,721,722,723,724,725,726(100p_OP) ,C717,718,719 (0.1u_OP) for EMI soluction
Modify 19: Change B38,B39 to 0 ohm 0805 size
Modify 20: Add R661,663(0 ohm),R662(0_OP),C727(0.1u_0603_OP),Q92.93.94.95(2n7002) and U46(A04422) for design issue
Modify 21: Change LAN power for S3 wakeup issue
Modify 22: Change R303(22K to 10K),R484(0 to 10K) and mount C632.634(0.1u_25V_X7R_0603) fo sequence issue
Modify 23: Add +3.3VS power plane for modem S3 wakeup issue
Modify 24: Change C201,204 from 10p to 18p for RTC issue
Modify 25: Change R216(22.6_1 to 20_1),R276,260(180 to 100),R214,233,263,270,268,271,257(220 TO 100) for design issue

R:B to R:B2 Change Note

Modify 26: Change +3.3V to +3.3VS for LED BD function
Modify 27: Change R299 from 0 to 200_1, C331 from 0.1u to 2.2u for thermal sensor power on sequence issue
Modify 28: No mount R194,R195,R204,R205 (4.7K) and change power plane from +5VA to +5V , change R442,R630 power plane from +3.3VA to +3.3V,change Q7,Q8 Gate power plane from +2.5V to +3.3V for design issue
Modify 29: Change R272 from 10K to 100K for S3 panel flash light issue
Modify 30: No mount C301,C302 (220P_OP) for SMBUS rise time issue
Modify 31: Change R196,R452 footprint to 0603 for 1/10W design issue
Modify 32: Mount C696,C609 and ADD C730 to 0.1u for EMI ESD fail soluction
Modify 33: Change R214,233,263,270,268,271,257(100 TO 47) for LED design issue
Modify 34: Add R671(47 ohm),C729(22p) for EMI request
Modify 35: Add R672(0_OP),change R156 from 100K to 0 ohm for EC request
Modify 36: Change Silent and Instant Pin to share with M30
Modify 37: Change C297,C298 and CON14 ,CON32 footprint for M/E request
Modify 38: Remove U21 circuit and Del C246,C251,C191,C186 (3900p) for unuse PATA HDD Spec
Modify 39: Change R216(20_1 to 18.7_1) for USB eye pattern issue
Modify 40: Add C41,C47,C731,C732,C733,C734,C735,D42,D43 for design issue
Modify 41: Add R673 and change R158 from 1K to 470 ohm for Safety issue
Modify 42: Add C736,C737,C738,C739,C740,C741,C742,C743,C744,C745,R674,R675,B43 and Del R668 for EMI
Modify 43: Del R653,R654,R656 and Add B44,B45,B46 for EMI

R:B2 to R:C Change Note

Modify 44: Del C211,C214,C422,C423 and Add C746,C747,C748,C749 for SATA link quality
Modify 45: Reserve C750 for EMI ESD function
Modify 46: Modify C343,C349,C176,C180,C142,C164,C322,C299,C5 footprint and Change R370,R367 from 820 to 953_1,C173 from 220p to 330p, mount C126,C143 (2200p) for design issue

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